REMARKS/ARGUMENTS

The Examiner's Action of August 12, 2004, has been received and reviewed by counsel for Assignee. Claims 33-43 were presented for examination, and all claims were rejected under Section 103 as unpatentable in view of *Guruswamy, et al.*, U.S. Patent 5,984,510, when combined with various other references as discussed below. In response to this Action counsel has amended certain claims, submits new claims herewith and offers the following remarks. As requested by the Examiner, counsel has canceled claims 1-32 and 44-64 as directed to nonelected inventions. These claims are the subject of divisional applications having Serial Nos. 10/925,252 and 10/925,061 in the U.S. Patent Office. As will be apparent, the references taken singly or in combination do not teach Applicant's claimed invention. Below is first discussed Applicant's invention, in summary, followed by a discussion of the prior art references.

The Telairity Technology

The technology developed by Applicant and Assignee as described herein approaches the design of integrated circuits in a different manner than was carried out before. The technology herein can be viewed as involving a two-step process for designing a finished integrated circuit. In a first operation, relatively large sub-circuits are designed all the way to a completed design. In other words, the sub-circuit is designed to the point of being a completed operational unit, for example, including the layout of the transistors and other components, the interconnecting wiring, and the ultimate shape that the circuit will have when manufactured as an integrated circuit. Two features of this approach are that when the sub-circuit is completely designed, it is used in subsequent designs in that form, and when completely designed, the interconnecting wiring does not use all of the layers available in the process technology which will ultimately be used to form the completed integrated circuit. Examples of such "groups" or "sub-circuits" are shown in Table 1 on page 9 of the application. An example as shown there is an 8-bit, twos-complement adder. As claimed in claim 1, these sub-circuits are then stored for later use in conjunction with other sub-circuits and other circuits. Then the integrated circuit itself is designed by retrieving these sub-circuits which have been previously optimized and stored, and using them in the design of the finished integrated circuit. The finished integrated circuit itself

typically will have from two to a large number of sub-circuits, as well as miscellaneous interconnecting logic which may not be in sub-circuit form, etc. The sub-circuits and the interconnecting logic are all connected together as desired using other layers in the integrated circuit process technology. This enables the design of the various units to be optimized to a relatively high degree for use in the completed integrated circuit. Importantly, it allows for the rapid design of relatively high performance integrated circuits.

In contrast, prior art solutions, such as described in the references cited, design and interconnect the resulting integrated circuit in a large operation involving optimization of large numbers of components, the design of large amounts of circuits, and the like. This results in extremely complex design and optimization problems, with the result of long lead time required for a design.

The Examiner's observation that the insurmountable job of designing a complex circuit by dividing it into smaller pieces is appreciated. Counsel, however, believes the primary benefit of the invention is the ability to re-use designs of sub-circuits in later projects. For example, once the 8-bit adder mentioned above is optimized, it may be re-used in any subsequent design without further redesign. This allows much faster and efficient design of integrated circuits.

Cited References

The primary reference, *Guruswamy, et al.*, typifies the prior art in the sense described above. That reference teaches a method for synthesizing standard cell layouts. A high level description of the process in *Guruswamy, et al.*, is shown in Figure 4 of that reference. As noted by the Examiner, *Guruswamy, et al.*, does not teach at least four elements of claim 33 presented herein. In particular, *Guruswamy, et al.*, does not teach:

> the first element of claim 33, creating a netlist for subcircuits having at least 300 gates;
>
> the third element claim 33 defining electrical connections on fewer than all available layers; and
>
> the last element of claim 33 defining desired electrical connections among the sub-circuits.

Counsel also believes that *Guruswamy, et al.*, does not teach many other elements of claim 33. For example, *Guruswamy, et al.*, does not teach the second element, creating a physical layout of each such sub-circuit. Because *Guruswamy, et al.*, does not teach designing sub-circuits having at least 300 gates, *Guruswamy, et al.*, does not define a layout for such a sub-circuit, which includes the limitation of claim 33 of defining "locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit." In *Guruswamy, et al.*, as counsel understands, the interconnections are not reduced in the manner claimed. In other words, according to the claimed invention, the number of interconnections to the sub-circuit is far fewer because all of the non-input/output connections can be ignored. Those interconnections are inside the sub-circuit and therefore are not important to other parts of the integrated circuit. In essence, in *Guruswamy, et al.*, all standard cells have interconnection points which allow them to be coupled to other standard cells. This results in a huge number of interconnection points. In contrast, in Applicant's invention, when the sub-circuit is defined, the interior interconnection points which are no longer needed for connection to other circuits "disappear" from the design. The only connections of concern are the "locations on each such sub-circuit for interconnecting such sub-circuit" to other circuits. Thus, for the reasons as discussed above, the design of the finished integrated circuit is simplified because the number of interconnection points is reduced.

Nor does *Guruswamy, et al.*, teach the fifth element of claim 33, optimizing the design of the sub-circuit to obtain "a desired level of operating speed for such sub-circuit independently of any use of such sub-circuit with any other sub-circuit." As shown by Figure 4 in *Guruswamy, et al.*, the analysis of circuit performance, step 158, is performed after all components are placed and the layout is compacted at step 156. The design optimization within *Guruswamy, et al.*, is discussed briefly in column 15 at lines 15-28. As described there, the optimization process is performed on the circuit as a whole, not on sub-circuits.

Nor does *Guruswamy, et al.*, teach the sixth element of claim 33, storing the optimized design for later use in conjunction with other sub-circuits. In *Guruswamy, et al.*, if a new circuit is designed, no use is made of previously-designed sub-circuits. A subsequent integrated circuit being designed using the methodology described in *Guruswamy, et al.*, would

employ the full process of the system described there, for example, as set forth in Figure 4. There is nothing in *Guruswamy, et al.*, which teaches the idea of saving a previously-designed and completed sub-circuit for later use in subsequent designs, as called out by claim 33 herein.

Guruswamy, et al., also fails to teach the seventh element of claim 33, creating a netlist which includes at least two sub-circuits previously optimized and stored.

For all of the reasons discussed above, it is clear that *Guruswamy, et al.*, makes no use of previously-designed integrated circuits, rather uses standard cells to design a new circuit each time a new circuit is desired. No reuse of previous large groups of circuitry is made.

Finally, with respect to claim 33, *Guruswamy, et al.*, also fails to each the eighth element, creating a physical layout by placing the sub-circuits on a design in proximity to each other. In *Guruswamy, et al.*, standard cells are used, and each integrated circuit is designed from such small units. New circuits are not designed using previously-designed and stored sub-circuits, and therefore *Guruswamy, et al.*, does not teach any step of placing sub-circuits on a design and using the previously-determined locations on each sub-circuit for interconnecting such sub-circuits with other circuits.

The Examiner has also cited *Crafts*, U.S. 5,671,397, and *Dangelo, et al.*, U.S. 5,880,971, as supplying some of the missing elements from *Guruswamy, et al.* It is first important to appreciate that neither of these references teaches the basic concept behind Applicant's invention in which the design of sub-circuits is performed and optimized and saved, and then later those sub-circuits are reused in larger designs to provide concomitant reduction in overall design time.

Dangelo, et al., does not provide any of the missing elements from *Guruswamy, et al.* The overall system in *Dangelo, et al.*, is shown in Figure 9. Note that the system operates entirely on a complete integrated circuit, and that no use appears to be made of previously-designed or optimized sub-circuits. As discussed in *Dangelo, et al.*, at colum 3, lines 45-58, the entire integrated circuit is simulated and then provided to a software system to define the physical implementation of the design. As mentioned there, this step appears to be a conventional one in the concept of *Dangelo, et al.*, in the sense that as described in column 3 at

lines 55-57, the design is provided to "existing software systems which control the physical implementation of the design, such as in an ASIC...."

The Examiner has cited *Dangelo, et al.*, as teaching circuit groups of less than a few thousand gates, citing column 13 at line 42. This does not appear to be an optimization of the actually-designed circuit, rather an estimator which provides estimates of wire delays which are later used by "the design compiler," which appears to mean the circuit design system. Note that the block level delay estimator 808 described in that paragraph is said to provide the benefit of "in pre-place and pre-layout stages of the design, both the synthesis and the analysis tool consider the wire delays to be a function of fan-out only." This suggests that the estimator is providing estimates on other bases (beyond fan-out only), <u>but in the pre-place and pre-layout stages of the design.</u>

In any event, nothing in the paragraph suggests the concept of designing sub-circuits, optimizing those sub-circuits, and then saving those sub-circuits for later reuse in subsequent designs. Rather, the paragraph is directed toward analysis of the design without regard to preexisting designs. Accordingly, *Dangelo, et al.*, is not believed to provide the missing teachings from *Guruswamy, et al.*, discussed above. It clearly does not create a physical layout for each sub-circuit which includes locations for connections to that sub-circuit, does not optimize the design of sub-circuits, store such optimized designs, create new integrated circuits which use at least two previously-designed sub-circuits, or create a physical layout in which the sub-circuits previously designed are used.

The *Crafts* reference, U.S. 5,671,397, is also cited by the Examiner. This reference describes a "sea-of-cells array of transistors and the wiring of such." It does not teach the numerous elements of claim 33 discussed above, not found in *Guruswamy, et al.*, or *Dangelo, et al.*

With respect to the dependent claims, the Examiner has cited the above references against selected ones of those claims. As suggested by the discussion above, while counsel may disagree with the characterizations of the references teaching various aspects of the dependent claims, because the references taken together do not teach all of the elements of the independent claim, all of the dependent claims herein are believed allowable for at least that reason.

Also presented herewith are new claims 65-72. These claims are believed to patentably distinguish the cited references for all of the reasons discussed above.

In view of the foregoing, counsel for Assignee believes all claims now pending in this application are in condition for allowance. The issuance of a Notice of Allowance is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, he is invited to telephone the undersigned at 650-326-2400.

Respectfully submitted,

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